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<input type="checkbox"/>	L10 (asynchronous\$4 near5 comput\$4 near5 digital near5 result)	2
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<input type="checkbox"/>	L8 L7 same asynchronous\$4	0
<input type="checkbox"/>	L7 L5 same (conver\$7 or translat\$7)	94
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L4: Entry 1 of 3

File: USPT

Apr 23, 2002

DOCUMENT-IDENTIFIER: US 6378011 B1

TITLE: Parallel to serial asynchronous hardware assisted DSP interface

Brief Summary Text (26):

The serial data module removes substantial overhead from the DSP by receiving parallel data reads and converting that data into asynchronous data frames to be sent out over the serial communication lines. The serial data module further optimizes communication between the DSP and the module by establishing flexible threshold values which allow the module to be optimized for a particular protocol and to take advantage of the high speed digital cellular networks. This flexibility is allows for the adaptation of the serial data module to various wireless communication protocols including AMPS cellular and digital cellular.

CLAIMS:

1. A serial data apparatus for converting parallel data generated by a digital signal processor (DSP) into asynchronous serial data bytes according to an asynchronous protocol specified by the DSP and in a separate pipeline converting asynchronous serial data to synchronous parallel data, the apparatus comprising:

a register module;

a receive data FIFO digitally connected to the register module;

a transmit data FIFO digitally connected to the register module;

a DSP interface digitally connected to the register module comprising a bidirectional control signal bus, a bidirectional DSP data bus, and a read only status bus;

a timing control interface digitally connected to the register module, the receive data FIFO, and the transmit FIFO;

a asynchronous serial data out (ASDO) pin digitally connected to the timing control interface; and

a asynchronous serial data in (ASDI) pin digitally connected to the timing control interface.

14. In a computer system including a modem with a parallel to serial asynchronous hardware assisted DSP interface, a method of communication that converts asynchronous digital cellular data into parallel synchronous data for the DSP and converts parallel synchronous data from the DSP into asynchronous serial data frames for transmission across a digital cellular communication line, the communication method comprising the steps of:

receiving asynchronous data into the interface and transmitting the data to the DSP in a parallel synchronous fashion;

receiving synchronous parallel data and sending the data in accordance with an

established asynchronous transfer rate and method;

said receiving asynchronous data into the interface and said transmitting data to the DSP step including the steps of:

receiving the asynchronous data from the digital cellular phone;

storing the data in a parallel fashion in a buffer until an appropriate threshold value is reached;

sending a threshold interrupt to the DSP;

reading parallel data a threshold number of times from the buffer;

said receiving synchronous data and said sending asynchronous data including the steps of:

writing a single parallel data byte to the interface;

placing the data in an interface buffer;

sending the data in accordance with an establish asynchronous protocol at an established transfer rate.

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L4: Entry 2 of 3

File: USPT

Oct 9, 1979

DOCUMENT-IDENTIFIER: US 4170714 A

**** See image for Certificate of Correction ****

TITLE: Digital cryptographic system and testing thereof

Brief Summary Text (9):

In accordance with another aspect of the present invention, a digital cryptographic system includes an array on a housing for inputting a plurality of different code variables. A memory is provided in the housing to store the code variables. A switch is provided on the housing to enable selection of any desired one of the stored code variables. A random code generator in the housing is responsive to the selected code variable for generating a stream of randomized key digital bits. Synchronous clear text digital data is applied to the housing, and enciphering circuitry therein enciphers the synchronous clear text digital data and generates an enciphered synchronous digital stream.

Drawing Description Text (17):

FIGS. 16a and 16b are schematic diagrams of the asynchronous converter shown in FIG. 2.

Detailed Description Text (22):

FIG. 2 is a block diagram of the present enciphering system. A data terminal 56 may comprise, for example, a conventional synchronous data terminal or the like for generating digital signals through the operation of a keyboard. The data terminal 56 is interconnected to the test circuitry 58, which performs the signal routing functions necessary to perform the system tests in connection with test switch 40 (FIG. 1), previously described. The test circuitry 58 may be interconnected to an optional external load 59. The test circuitry 58 may also be connected to an asynchronous converter 60, which converts asynchronous data to synchronous data in the receive mode of operation of unit 10 and synchronous data to asynchronous data in the send mode of operation of unit 10. The asynchronous converter 60 provides unit 10 with the additional capability of receiving asynchronous data.

Detailed Description Text (23):

If the asynchronous converter 60 is not utilized, the test circuitry 58 is directly connected to the interface logic 62 of the present enciphering system. Interface logic 62 is also connected to a data modem 64 through the test circuitry 58. The data modem 64 may comprise any suitable conventional synchronous data modem. The output of the data modem 64 is applied to a data link such as a teleprinter transmission line or the like. The interface logic 62 of the present system is applied to control logic 66, which acts to control the various functions of the system. The key variable storage 68 contains memories for storing the codes input to the unit 10 via the push-button switches 20 in the manner previously described.

Detailed Description Text (26):

In operation of the present system, digital signals are applied from the data terminal 56 through the test circuitry 58 to either the asynchronous converter 60 or directly to the interface logic 62. The interface logic 62 converts the data terminal signals to standard logic levels and operates on these logic levels to produce control signals for application to the control logic 66. The control logic 66 operates to encipher the data in accordance with the key variables stored in key

variable storage 68 and code generator send 80. The control logic 66 then transmits the enciphered data through the interface logic 62 to the data modem 64 through the asynchronous converter 60, if asynchronous data is desired, and the test circuitry 58. The interface logic 62 converts logic signals to standard digital signals according to EIA specification for interfacing to digital equipment. The present circuitry also includes synchronization and correlation circuitry which will be subsequently described in greater detail. The system operates to decipher data obtained from the data modem 64 in the reverse manner.

Detailed Description Text (152):

Asynchronous Converter

Detailed Description Text (153):

Referring now to FIGS. 16a and 16b, the circuitry comprising the asynchronous converter represented by block 60 in FIG. 2 is shown. FIGS. 16a and 16b are drawn to be matched in a side-by-side relationship to illustrate the entire electrical schematic. As previously stated, the asynchronous converter 60 is interconnected between the test circuitry 58 and interface logic 62 (FIG. 2). The asynchronous converter 60 functions to convert asynchronous data from the data terminal 56 to synchronous data for utilization by the interface logic 62, and functions to convert synchronous data from the interface logic 62 to asynchronous data for utilization by the data terminal 56.

Detailed Description Text (154):

Referring to FIG. 16a, the circuitry for converting asynchronous data to synchronous data is illustrated. The TBA signal in the form of asynchronous data is applied from the data terminal 56 (FIG. 2) to a receiver 1180. Receiver 1180 may comprise, for example, a 75154 I/C. Receiver 1180 is interconnected to a flip-flop 1182 through inverter 1184. Receiver 1180 is also interconnected to flip-flop 1182 through NAND gates 1186 and 1187. The output of flip-flop 1182 is applied to flip-flops 1188 and 1190. The output of flip-flop 1190 is interconnected to NAND gate 1186 through AND gate 1192.

Detailed Description Text (155):

The asynchronous data through inverter 1184 is also applied to a shift register 1194, which is interconnected to a shift register 1196. Shift registers 1194 and 1196 are four stage static shift registers and may comprise, for example, 4015 I/Cs. The outputs of shift registers 1194 and 1196 are applied to a shift register 1198. Shift register 1198 is an eight bit shift register and may comprise, for example, a 4021 I/C. The output of register 1198 is applied to a multiplexer 1200. Multiplexer 1200 is a dual four channel select multiplexer and may comprise, for example, a 4539 I/C. The output of multiplexer 1200 is applied to a flip-flop 1202, which is interconnected to a flip-flop 1204. The output of flip-flop 1204 is applied to the "X" input of a multiplexer 1206. Multiplexer 1206 is a four bit AND/OR selector multiplexer and may comprise, for example, a 4519 I/C. The output of multiplexer 1206 is applied through inverter 1208 to a driver 1210. Driver 1210 is a dual line driver and may comprise, for example, a 75150 I/C. Driver 1210 generates the TBA* output signal, which represents synchronous data converted from the TBA asynchronous input data.

Detailed Description Text (156):

The asynchronous converter 60 may also be utilized to route synchronous data through converter 60 to the interface logic 62. If the TBA signal was synchronous data initially, the output of inverter 1184 would apply this synchronous data to the "Y" input of multiplexer 1206. The output of driver 1210 would, therefore, represent synchronous data applied to the interface logic 62. A mode select switch 1212 is utilized to select either the "X" or "Y" inputs to multiplexer 1206 depending upon whether the input data is asynchronous or synchronous. Mode select switch 1212 in the open position programs the converter 60 to receive asynchronous data and, therefore, the X input to multiplexer 1206 is selected. Mode select

switch 1212 in the closed position programs the converter 60 to receive synchronous data, which is applied to the Y input of multiplexer 1206. Select switch 1212 is interconnected to an inverter 1214, which is interconnected to a multiplexer 1216. Multiplexer 1216 is a four bit AND/OR selector multiplexer and may comprise, for example, a 4519 I/C.

Detailed Description Text (161):

The number of bits per character of the asynchronous data must also be preselected depending upon the type of asynchronous data being converted by the converter 60. There may be 8, 9, 10 or 11 bits per character of asynchronous data and this information is preprogrammed by operation of switches 1230a and 1230b. The positioning of switches 1230a and 1230b is determined by the number of bits per character selected. For a typical number of bits per character, the switch positions of switches 1230a and 1230b are tabulated in Table 2 below.

Detailed Description Text (162):

Once selected, the number of bits per character is applied via signal lines A and B to multiplexer 1232. Multiplexer 1232 is a four channel select/multiplexer and may comprise, for example, a 4539 I/C. The asynchronous data rate generated at the output of counter 1228 is applied to a counter 1234. Counter 1234 is a dual binary up counter and may comprise, for example, a 4520 I/C. The output of counter 1234 is applied through AND gate 1236 to a shift register 1238 and through an inverter 1237 to counter 1234. Shift register 1238 is a dual four stage static register and may comprise, for example, a 4015 I/C. The output of shift register 1238 is applied to multiplexer 1232 to generate an output signal which signifies that a completed character of asynchronous data has been received by the converter 60.

Detailed Description Text (165):

The request to send signal TCA is applied to a driver 1260 which is interconnected to a driver 1262. Driver 1262 is interconnected to AND gate 1264, which supplies its output to flip-flop 1226, counter 1228, and through inverter 1265 and NAND gate 1265a to counters 1220 and 1222. Driver 1262 is also interconnected to a counter 1266, which through inverter 1268 is interconnected to a flip-flop 1270. The output of flip-flop 1270 is applied to the "X" input of a multiplexer 1272. The output of multiplexer 1272 is interconnected through an inverter 1274 to a driver 1276 to generate the TCA* output signal. The output of flip-flop 1270 is applied to the "X" input of multiplexer 1272. If the mode select switch 1212 is in the open position, the converter receives asynchronous data. If synchronous data is received by the converter 60, mode select switch 1212 is closed so that the TCA signal is then applied to the "Y" input of multiplexer 1272 to be merely routed through the converter 60 as synchronous data.

Detailed Description Text (166):

To summarize the conversion from asynchronous to synchronous data performed by asynchronous converter 60, mode select switch 1212 is placed in the open position, switches 1218 are positioned to generate the desired asynchronous data rate and switches 1230 are positioned to generate the desired number of bits per character of the asynchronous data. Upon receipt of a request to send TCA signal the output of receiver 1262 is applied to the input of flip-flop 1182. Upon receipt of the leading edge of the start bit of asynchronous carrier, flip-flop 1182 is set and flip-flops 1188 and 1190 are reset. If the data has gone to a zero level halfway through a bit, flip-flops 1188 and 1190 produce a reset and shut flip-flop 1182 off. The purpose of this reset is to prevent noise from being received and then converted to meaningless data by the converter 60. Flip-flops 1188 and 1190 comprise a false start detector circuit which interrogates the data line to insure that it is at a zero level. If the data line is not at a zero level, flip-flops 1188 and 1190 will generate a reset pulse to reset flip-flop 1182. Assuming that no reset is necessary, the asynchronous data gets clocked into the shift registers 1194 and 1196. The number of data bits clocked into these shift registers is determined by the position of switches 1230a and 1230b which determine the number

of bits per character.

Detailed Description Text (168):

Referring to FIG. 16b, the circuitry representing the receive portion of the asynchronous converter 60 is shown. This circuitry receives the TBB* signal in synchronous form and converts this data to the TBB signal as asynchronous applied to the data modem 64 (FIG. 2). The TBB* signal is applied through a receiver 1290 to shift registers 1292 and 1294. Shift registers 1292 and 1294 are dual four stage static registers and may comprise, for example, 4015 I/Cs. The output of shift register 1294 is applied to a flip-flop 1296, whose output is applied to a flip-flop 1298. The asynchronous start bit will be applied to flip-flop 1298 to begin the clocking process. Flip-flop 1298 is interconnected to a shift register 1300, which also receives the CGC signal.

Detailed Description Text (170):

Latches 1316 and 1318 are interconnected to a shift register 1322 whose output is applied to a flip-flop 1324. The output of flip-flop 1324 is applied to the "X" input of a multiplexer 1326. Multiplexer 1326 is a four bit AND/OR selector multiplexer and may comprise, for example, a 4519 I/C. The output of multiplexer 1326 is applied through an inverter 1328 to a driver 1330 to generate the TBB output signal, which is asynchronous converted data. If mode select switch 1212 (FIG. 16a) was in the closed position, the synchronous data would be applied from the output of receiver 1290 through an inverter 1291 to the "Y" input of multiplexer 1326 for routing through converter 60.

Detailed Description Text (171):

The switches 1218a-1218g (FIG. 16a) are interconnected to counters 1332 and 1334 along signal lines a-g. Counters 1332 and 1334 are programmable divide-by-N four bit counters and may comprise, for example, 4526 I/Cs. Counter 1332 receives the CGC, 961,200 Hz fast clock signal, and has an output through inverter 1336 to flip-flop 1338. The output of flip-flop 1338 is applied to a counter 1340. Counters 1332, 1334 and 1340 together with flip-flop 1338 comprise a counter chain similar to counters 1220, 1222 and 1228 and flip-flop 1226 (FIG. 16a) of the synchronous to asynchronous conversion portion of converter 60. An independent counter chain is required for the synchronous to asynchronous conversion performed by the circuitry of FIG. 16b and is operable to clock the data out of counter 1322 to flip-flop 1324.

Detailed Description Text (175):

Operation of the present system will now be summarized utilizing the circuitry previously described. For simplicity of discussion, it will be assumed that the asynchronous converter 60 is not utilized. The asynchronous converter 60 when used merely functions to perform a data conversion between the data terminal 66, interface logic 62 and data modem 64. The test circuitry 58 can be considered to be directly connected to the interface logic 62. In this discussion, it will also be assumed that all system tests have been conducted utilizing switch 40 (FIG. 1), therefore, the test circuitry 50 merely performs a routing function between the data terminal 56 and interface logic 62 and between interface logic 62 and the data modem 64.

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L4: Entry 3 of 3

File: USPT

Jan 9, 1979

DOCUMENT-IDENTIFIER: US 4133973 A

**** See image for Certificate of Correction ****

TITLE: Digital cryptographic system having synchronous and asynchronous capabilities

Brief Summary Text (9):

In accordance with another aspect of the present invention, a digital cryptographic system includes an array on a housing for inputting a plurality of different code variables. A memory is provided in the housing to store the code variables. A switch is provided on the housing to enable selection of any desired one of the stored code variables. A random code generator in the housing is responsive to the selected code variable for generating a stream of randomized key digital bits. Synchronous clear text digital data is applied to the housing, and enciphering circuitry therein enciphers the synchronous clear text digital data and generates an enciphered synchronous digital stream.

Drawing Description Text (17):

FIGS. 16a and 16b are schematic diagrams of the asynchronous converter shown in FIG. 2.

Detailed Description Text (22):

FIG. 2 is a block diagram of the present enciphering system. A data terminal 56 may comprise, for example, a conventional synchronous data terminal or the like for generating digital signals through the operation of a keyboard. The data terminal 56 is interconnected to the test circuitry 58, which performs the signal routing functions necessary to perform the system tests in connection with test switch 40 (FIG. 1), previously described. The test circuitry may be interconnected to an optional external load 59. The test circuitry 58 may also be connected to an asynchronous converter 60, which converts asynchronous data to synchronous data in the receive mode of operation of unit 10 and synchronous data to asynchronous data in the send mode of operation of unit 10. The asynchronous converter 60 provides unit 10 with the additional capability of receiving asynchronous data.

Detailed Description Text (23):

If the asynchronous converter 60 is not utilized, the test circuitry 58 is directly connected to the interface logic 62 of the present enciphering system. Interface logic 62 is also connected to a data modem 64 through the test circuitry 58. The data modem 64 may comprise any suitable conventional synchronous data modem. The output of the data modem 64 is applied to a data link such as a teleprinter transmission line or the like. The interface logic 62 of the present system is applied to control logic 66, which acts to control the various functions of the system. The key variable storage 68 contains memories for storing the codes input to the unit 10 via the pushbutton switches 20 in the manner previously described.

Detailed Description Text (26):

In operation of the present system, digital signals are applied from the data terminal 56 through the test circuitry 58 to either the asynchronous converter 60 or directly to the interface logic 62. The interface logic 62 converts the data

terminal signals to standard logic levels and operates on these logic levels to produce control signals for application to the control logic 66. The control logic 66 operates to encipher the data in accordance with the key variables stored in key variable storage 68 and code generator send 80. The control logic 66 then transmits the enciphered data through the interface logic 62 to the data modem 64 through the asynchronous converter 60, if asynchronous data is desired, and the test circuitry 58. The interface logic 62 converts logic signals to standard digital signals according to EIA specification for interfacing to digital equipment. The present circuitry also includes synchronization and correlation circuitry which will be subsequently described in greater detail. The system operates to decipher data obtained from the data modem 64 in the reverse manner.

Detailed Description Text (152):

ASYNCHRONOUS CONVERTER

Detailed Description Text (153):

Referring now to FIGS. 16a and 16b, the circuitry comprising the asynchronous converter represented by block 60 in FIG. 2 is shown. FIGS. 16a and 16b are drawn to be matched in a side-by-side relationship to illustrate the entire electrical schematic. As previously stated, the asynchronous converter 60 is interconnected between the test circuitry 58 and interface logic 62 (FIG. 2). The asynchronous converter 60 functions to convert asynchronous data from the data terminal 56 to synchronous data for utilization by the interface logic 62, and functions to convert synchronous data from the interface logic 62 to asynchronous data for utilization by the data terminal 56.

Detailed Description Text (154):

Referring to FIG. 16a, the circuitry for converting asynchronous data to synchronous data is illustrated. The TBA signal in the form of asynchronous data is applied from the data terminal 56 (FIG. 2) to a receiver 1180. Receiver 1180 may comprise, for example, a 75154 I/C. Receiver 1180 is interconnected to a flip-flop 1182 through inverter 1184. Receiver 1180 is also interconnected to flip-flop 1182 through NAND gates 1186 and 1187. The output of flip-flop 1182 is applied to flip-flops 1188 and 1190. The output of flip-flop 1190 is interconnected to NAND gate 1186 through AND gate 1192.

Detailed Description Text (155):

The asynchronous data through inverter 1184 is also applied to a shift register 1194, which is interconnected to a shift register 1196. Shift registers 1194 and 1196 are four stage static shift registers and may comprise, for example, 4015 I/Cs. The outputs of shift registers 1194 and 1196 are applied to a shift register 1198. Shift register 1198 is an eight bit shift register and may comprise, for example, a 4021 I/C. The output of register 1198 is applied to a multiplexer 1200. Multiplexer 1200 is a dual four channel select multiplexer and may comprise, for example, a 4539 I/C. The output of multiplexer 1200 is applied to a flip-flop 1202, which is interconnected to a flip-flop 1204. The output of flip-flop 1204 is applied to the "X" input of a multiplexer 1206. Multiplexer 1206 is a four bit AND/OR selector multiplexer and may comprise, for example, a 4519 I/C. The output of multiplexer 1206 is applied through inverter 1208 to a driver 1210. Driver 1210 is a dual line driver and may comprise, for example, a 75150 I/C. Driver 1210 generates the TBA* output signal, which represents synchronous data converted from the TBA asynchronous input data.

Detailed Description Text (156):

The asynchronous converter 60 may also be utilized to route synchronous data through converter 60 to the interface logic 62. If the TBA signal was synchronous data initially, the output of inverter 1184 would apply this synchronous data to the "Y" input of multiplexer 1206. The output of driver 1210 would, therefore, represent synchronous data applied to the interface logic 62. A mode select switch 1212 is utilized to select either the "X" or "Y" inputs to multiplexer 1206

depending upon whether the input data is asynchronous or synchronous. Mode select switch 1212 in the open position programs the converter 60 to receive asynchronous data and, therefore, the X input to multiplexer 1206 is selected. Mode select switch 1212 in the closed position programs the converter 60 to receive synchronous data, which is applied to the Y input of multiplexer 1206. Select switch 1212 is interconnected to an inverter 1214, which is interconnected to a multiplexer 1216. Multiplexer 1216 is a four bit AND/OR selector multiplexer and may comprise, for example, a 4519 I/C.

Detailed Description Text (161):

The number of bits per character of the asynchronous data must also be preselected depending upon the type of asynchronous data being converted by the converter 60. There may be 8, 9, 10 or 11 bits per character of asynchronous data and this information is preprogrammed by operation of switches 1230a and 1230b. The positioning of switches 1230a and 1230b is determined by the number of bits per character selected. For a typical number of bits per character, the switch positions of switches 1230a and 1230b are tabulated in Table 2 below.

Detailed Description Text (162):

Once selected, the number of bits per character is applied via signal lines A and B to multiplexer 1232. Multiplexer 1232 is a four channel select/multiplexer and may comprise, for example, a 4539 I/C. The asynchronous data rate generated at the output of counter 1228 is applied to a counter 1234. Counter 1234 is a dual binary up counter and may comprise, for example, a 4520 I/C. The output of counter 1234 is applied through AND gate 1236 to a shift register 1238 and through an inverter 1237 to counter 1234. Shift register 1238 is a dual four stage static register and may comprise, for example, a 4015 I/C. The output of shift register 1238 is applied to multiplexer 1232 to generate an output signal which signifies that a completed character of asynchronous data has been received by the converter 60.

Detailed Description Text (165):

The request to send signal TCA is applied to a driver 1260 which is interconnected to a driver 1262. Driver 1262 is interconnected to AND gate 1264, which supplies its output to flip-flop 1226, counter 1228, and through inverter 1265 and NAND gate 1265a to counters 1220 and 1222. Driver 1262 is also interconnected to a counter 1266, which through inverter 1268 is interconnected to a flip-flop 1270. The output of flip-flop 1270 is applied to the "X" input of a multiplexer 1272. The output of multiplexer 1272 is interconnected through an inverter 1274 to a driver 1276 to generate the TCA* output signal. The output of flip-flop 1270 is applied to the "X" input of multiplexer 1272. If the mode select switch 1212 is in the open position, the converter receives asynchronous data. If synchronous data is received by the converter 60, mode select switch 1212 is closed so that the TCA signal is then applied to the "Y" input of multiplexer 1272 to be merely routed through the converter 60 as synchronous data.

Detailed Description Text (166):

To summarize the conversion from asynchronous to synchronous data performed by asynchronous converter 60, mode select switch 1212 is placed in the open position, switches 1218 are positioned to generate the desired asynchronous data rate and switches 1230 are positioned to generate the desired number of bits per character of the asynchronous data. Upon receipt of a request to send TCA signal the output of receiver 1262 is applied to the input of flip-flop 1182. Upon receipt of the leading edge of the start bit of asynchronous carrier, flip-flop 1182 is set and flip-flops 1188 and 1190 are reset. If the data has gone to a zero level halfway through a bit, flip-flops 1188 and 1190 produce a reset and shut flip-flop 1182 off. The purpose of this reset is to prevent noise from being received and then converted to meaningless data by the converter 60. Flip-flops 1188 and 1190 comprise a false start detector circuit which interrogates the data line to insure that it is at a zero level. If the data line is not at a zero level, flip-flops 1188 and 1190 will generate a reset pulse to reset flip-flop 1182. Assuming that no

reset is necessary, the asynchronous data gets clocked into the shift registers 1194 and 1196. The number of data bits clocked into these shift registers is determined by the position of switches 1230a and 1230b which determine the number of bits per character.

Detailed Description Text (168):

Referring to FIG. 16b, the circuitry representing the receive portion of the asynchronous converter 60 is shown. This circuitry receives the TBB* signal in synchronous form and converts this data to the TBB signal as asynchronous applied to the data modem 64 (FIG. 2). The TBB* signal is applied through a receiver 1290 to shift registers 1292 and 1294. Shift registers 1292 and 1294 are dual four stage static registers and may comprise, for example, 4015 I/Cs. The output of shift register 1294 is applied to a flip-flop 1296, whose output is applied to a flip-flop 1298. The asynchronous start bit will be applied to flip-flop 1298 to begin the clocking process. Flip-flop 1298 is interconnected to a shift register 1300, which also receives the CGC signal.

Detailed Description Text (170):

Latches 1316 and 1318 are interconnected to a shift register 1322 whose output is applied to a flip-flop 1324. The output of flip-flop 1324 is applied to the "X" input of a multiplexer 1326. Multiplexer 1326 is a four bit AND/OR selector multiplexer and may comprise, for example, a 4519 I/C. The output of multiplexer 1326 is applied through an inverter 1328 to a driver 1330 to generate the TBB output signal, which is asynchronous converted data. If mode select switch 1212 (FIG. 16a) was in the closed position, the synchronous data would be applied from the output of receiver 1290 through an inverter 1291 to the "Y" input of multiplexer 1326 for routing through converter 60.

Detailed Description Text (171):

The switches 1218a-1218g (FIG. 16a) are interconnected to counters 1332 and 1334 along signal lines a-g. Counters 1332 and 1334 are programmable divide-by-N four bit counters and may comprise, for example, 4526 I/Cs. Counter 1332 receives the CGC, 961,200 Hz fast clock signal, and has an output through inverter 1336 to flip-flop 1338. The output of flip-flop 1338 is applied to a counter 1322. Counters 1332, 1334 and 1340 together with flip-flop 1338 comprise a counter chain similar to counters 1220, 1222 and 1228 and flip-flop 1226 (FIG. 16a) of the synchronous to asynchronous conversion portion of converter 60. An independent counter chain is required for the synchronous to asynchronous conversion performed by the circuitry of FIG. 16b and is operable to clock the data out of counter 1322 to flip-flop 1324.

Detailed Description Text (175):

Operation of the present system will now be summarized utilizing the circuitry previously described. For simplicity of discussion, it will be assumed that the asynchronous converter 60 is not utilized. The asynchronous converter 60 when used merely functions to perform a data conversion between the data terminal 66, interface logic 62 and data modem 64. The test circuitry 58 can be considered to be directly connected to the interface logic 62. In this discussion, it will also be assumed that all system tests have been conducted utilizing switch 40 (FIG. 1), therefore, the test circuitry 50 merely performs a routing function between the data terminal 56 and interface logic 62 and between interface logic 62 and the data modem 64.

CLAIMS:

8. The digital cryptographic system of claim 7 wherein said clear text digital data is generated from a synchronous terminal source.

19. A digital cryptographic system for enciphering asynchronous clear text digital data transmitted from a data terminal through a modem to a receiving station,

comprising:

circuitry for receiving a request signal from the data terminal and for inputting said request signal through the modem in order to synchronize the modem,

means responsive to a clear to send signal generated by the modem upon synchronization thereof for generating prime and synchronization signals and for inputting said prime and synchronization signals to the modem for transmission to the receiving station,

means responsive to the synchronization of the receiving station for generating a clear to send signal and for transmitting said clear to send signal to the terminal to enable the asynchronous clear text digital data to be input through said cryptographic system,

means for converting the asynchronous clear text digital data from the data terminal to synchronous clear text digital data,

means for synchronously enciphering the converted asynchronous clear text digital data,

means for converting the synchronously enciphered converted asynchronous clear text digital data to synchronous enciphered digital data, and

means for transmitting the enciphered digital data to the modem for transmission to the receiving station.

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L10: Entry 1 of 2

File: USPT

Feb 19, 1991

DOCUMENT-IDENTIFIER: US 4995040 A

TITLE: Apparatus for management, comparison, and correction of redundant digital data

Brief Summary Text (19):

The present invention is a system for controlling and managing redundant inter-processor communication channels. The system comprises two major components, a Dual-Port Message Buffer and a Redundancy Management Unit. These components provide hardware support for synchronization of redundant, distributed, asynchronous digital computers; comparison of computational results from the redundant computers; and correction of faults detected by means of a majority vote mechanism.

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L10: Entry 2 of 2

File: DWPI

Aug 8, 1990

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DERWENT-WEEK: 199032

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TITLE: Management comparison and correction of redundant digital data - has dual-port message buffer with RAM for storage and redundancy management unit to control data elements

Basic Abstract Text (1):

The system controls and manages redundant inter-processor communication channels. The system comprises two major components, a Dual-Port Message Bufer and a Redundancy Management Unit. These components provide hardware support for synchronisation or redundant, distributed, asynchronous digital computers; comparison of computational results from the redundant computers; and correction of faults detected by means of a majority vote mechanism. The Dual-Port Message Buffer (DPB) comprises a dual-port random access memory (RAM) which stores a multiplicity of messages that are received asynchronously over a communication channel. Received messages are stored through the first port of the dual-port RAM and removed for processing through the second port. For a given computer, each independent communication channel is serviced by a dedicated DPB.

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